IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Harinath B. Kamepalli, Padmaraj Sanjeevarao, Chang-Jin Park		
Assignee:	Sun Microsystems, Inc.		
Title:	Scan Chain Verification Using Symbolic Simulation		
Serial No.:	10/790,650	Filed:	March 1, 2004
Examiner:	Unknown	Group Art Unit:	Unknown
Docket No.:	SUN040292	Customer No.:	33438

Austin, Texas
April 28, 2004

COMMISSIONER FOR PATENTS
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Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, Applicants wish to call the following documents to the attention of the Examiner.

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, PO Box 1450, Alexandria, VA 22313-1450, on April 28, 2004.

Attorney for Applicant(s) — Date of Signature: 4/28/04

Respectfully submitted,

Michael Rocco Cannatti
Attorney for Applicant(s)
Reg. No. 34,791

U.S. Department of Commerce, Patent and Trademark Office	Attorney Docket No.	Serial No.
	SUN040292	10/790,650
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Harinath B. Kamepalli et al.	
	Filing Date	Group
	March 1, 2004	Unknown

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,634,012	10/14/2003	Zhong et al.	716	5	
	AB	6,631,470	10/07/2003	Chang et al.	713	3	
	AC	6,574,762	06/03/2003	Karimi et al.	714	727	
	AD	6,327,687	12/04/2001	Rajski et al.	714	738	
	AE	6,134,689	10/17/2000	Mateja et al.	714	736	
	AF	2003/0204802A1	10/30/2003	Sim	714	726	
	AG	2003/0131298A1	07/10/2003	Rajski et al.	714	738	
	AH	2003/0065996A1	04/03/2003	Shimada et al.	714	718	
	AI	2002/0053057A1	05/02/2002	Rajski et al.	714	738	
	AJ						
	AK						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL						☐	☐
	AM						☐	☐
	AN						☐	☐
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	Takahashi, Tsuyoshi, et al., "Design Flow and Design Environment for System LSIs," Hitachi Review Vol. 48 (1999) No. 2, pp. 87-93
	AS	Kurup, Pran, et al., "Mastering HDL for formal verification," Electronics Engineer, May 1999
	AT	http://www.stridge.com/Stridge_articles/atpg_model_oview.html, "Memory ATPG Modeling and Validation Process"

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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		Document	Date	Country	Class	Subclass	Yes	No
	AL						☐	☐
	AM						☐	☐
	AN						☐	☐
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	http://www.synopsys.com/products/acmgr/innlo/, "Former InnoLogic Systems Products"
	AS	http://www.synopsys.com/products/acmgr/innlo/espcv.html, "ESP-CV"
	AT	http://www.synopsys.com/products/acmgr/innlo/esplv.html, "ESP-LV"

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Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL						☐	☐
	AM						☐	☐
	AN						☐	☐
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	http://www.synopsys.com/products/acmgr/innlo/espbv.html, "ESP-BV"
	AS	http://www.synopsys.com/products/acmgr/innlo/ckt.html, "CKT"
	AT	http://www.synopsys.com/products/acmgr/innlo/casestudy/suncase.html, "Case Study"

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